

What is claimed is:

1. A timing extraction circuit which uses a PLL circuit containing a phase comparator circuit for performing a phase comparison between a data signal of
5 bit rate B (bits/s) and a clock signal of $B/2$ (Hz) at intervals of $2/B$ (sec), said timing extraction circuit comprising:

a detection circuit for detecting the absence of an output of phase comparison information from
10 said phase comparator circuit by receiving a data signal of a prescribed pattern; and

a control circuit for controlling, upon detecting said absence, the phase of said clock signal in order to maintain synchronization.

15 2. A circuit as claimed in claim 1, wherein said control circuit controls the phase of said clock signal by inverting said clock signal.

3. A circuit as claimed in claim 1, wherein said control circuit controls the phase of said clock signal
20 by controlling a VCO.

4. A timing extraction circuit which uses a PLL circuit containing a phase comparator circuit for performing a phase comparison between a data signal of
25 bit rate B (bits/s) and a clock signal of $B/2$ (Hz) at intervals of $2/B$ (sec), wherein said phase comparator circuit comprises two phase comparator circuits which respectively accept phases differing by one cycle ($1/B$ sec) of said data signal to perform phase comparisons for all data signals.

30 5. A duty cycle deviation handling circuit for use in an optical receiver, comprising:

a PLL circuit containing a phase comparator circuit for performing a phase comparison between a data signal of bit rate B (bits/s) and a clock
35 signal of $B/2$ (Hz) at intervals of $2/B$ (sec);

a duty cycle evaluation circuit for evaluating a duty cycle between input data before and

after a point at which said PLL circuit is locked; and
a control circuit for controlling, based
on a result of said evaluation, a data discrimination
phase before and after the point at which said PLL
5 circuit is locked.

6. A circuit as claimed in claim 5, wherein
said control circuit includes an initial
phase setting circuit in which duty cycle information
representing an initial phase adjustment is set, and
10 said initial phase setting circuit
compares said duty cycle information representing said
initial phase adjustment with an output of said duty
cycle evaluation circuit and, when locked in phase in the
same condition as said duty cycle information
15 representing said initial phase adjustment, said locked
condition is maintained, but when locked in phase in a
condition different from said duty cycle information
representing said initial phase adjustment, a clock
output of a voltage-controlled oscillator in said PLL
20 circuit is inverted.

7. A circuit as claimed in claim 5, wherein
said PLL circuit discriminates said input
data every other bit by using said clock signal whose
frequency is equal to one half the data transmission rate
25 and an inverted version of said clock signal, and
achieves a phase lock in accordance with a result
obtained by exclusive-ORing the data discriminated by a
clock signal delayed in phase by one half cycle of said
data signal with the data discriminated by said half-
30 frequency clock signal and the data discriminated by the
inverted version of said half-frequency clock signal,
respectively, and by comparing average values of said
respective exclusive-OR sums,

said duty cycle evaluation circuit
35 evaluates said duty cycle to determine whether said duty
cycle changes from "narrow" to "wide" or from "wide" to
"narrow" between said input data before and after the

point at which said PLL circuit is locked, said evaluation being made based on a result obtained by exclusive-ORing the data discriminated by an inverted version of said clock signal delayed in phase by one half
5 cycle of said data signal with the data discriminated by said half-frequency clock signal and the inverted version of said half-frequency clock signal, respectively, and by comparing average values of said respective exclusive-OR sums, and

10 said control circuit, based on the result of said evaluation, controls the phase of said clock signal delayed in phase by one half cycle of said data signal and the phase of the inverted version of said clock signal respectively in opposite directions.

15 8. A circuit as claimed in claim 7, wherein the discrimination phases of said clock signal and the inverted version thereof for discriminating said data signal are adjusted independently of each other by adjusting the phase of said clock signal independently of
20 the phase of said clock signal delayed in phase by one half cycle of said data signal.